QUEUE CIRCUIT AND METHOD FOR MEMORY ARBITRATION EMPLOYING SAME

ABSTRACT OF THE DISCLOSURE

A memory access arbitration scheme is provided where transactions to a shared memory are stored in an arbitration queue. A collapsible queuing structure and method are provided, such that once a transaction is serviced, higher order entries ripple down in the queue to make room for new entries while maintaining an oldest to newest relationship among the queue entries. A queuing circuit having a plurality of registers interconnected by 2:1 multiplexers is also provided. The circuit is arranged such that each register receives either its own current contents or the contents of a higher order register during each register write cycle.